

[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alt](#)

Welcome United States Patent and Trademark Office

☐ Search Results[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "((ddr <and> clock <near/5> phase)<in>metadata)"

Your search matched 3 of 1144315 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

[e-mail](#)[» View Session History](#)[» New Search](#)[» Key](#)

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Modify Search

☐ Check to search only within this results setDisplay Format: ☒ Citation ☐ Citation & Abstract

Select Article Information

- ☐
1. Synchronous mirror delay for multiphase locking
Yong Jin Yoon; Hyuck In Kwon; Jong Duk Lee; Byung Gook Park; Nam Seog Kim; Uk Rae Cho; Hyun Guen I
Solid-State Circuits, IEEE Journal of
Volume 39, Issue 1, Jan. 2004 Page(s):150 - 156
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(512 KB) IEEE JNL
- ☐
2. A delay-locked loop and 90-degree phase shifter for 100 Mbps double data rate memories
Yoshimura, T.; Nakase, Y.; Watanabe, N.; Morooka, Y.; Matsuda, Y.; Kumano, M.; Hamano, H.;
VLSI Circuits, 1998. Digest of Technical Papers. 1998 Symposium on
11-13 June 1998 Page(s):66 - 67
[AbstractPlus](#) | Full Text: [PDF](#)(228 KB) IEEE CNF
- ☐
3. A low jitter, fast recoverable, fully analog DLL using tracking ADC for high speed and low stand-by power interface
Se Jun Kim; Sang Hoon Hong; Jae-Kyung Wee; Jin Hong Ahn; Jin Young Chung;
VLSI Circuits, 2003. Digest of Technical Papers. 2003 Symposium on
12-14 June 2003 Page(s):285 - 286
[AbstractPlus](#) | Full Text: [PDF](#)(264 KB) IEEE CNF

[Help](#) [Contact Us](#) [Privacy](#)

© Copyright 2005 IE

Indexed by

